Method of forming an electrostatic discharge protecting device and integrated circuit arrangement comprising such a device

A simple and cost-effective method to improve ESD performance by selectively reducing avalanche breakdown voltage in protection devices by means of locally increasing the acceptor dopant concentration.

The present invention relates to a method of forming on a semiconductor substrate an electrostatic discharge (ESD) protecting device together with internal circuitry to be protected by the protecting device. Furthermore, the present invention relates to an integrated circuit arrangement comprising such an ESD protecting device and internal circuitry.

With advances in the development of high density very large scale integration (VLSI) circuits, the dimensions of the devices continue to shrink resulting in a corresponding decrease in the gate oxide thicknesses and junction depths in CMOS (Complementary Metal Oxide Semiconductor) devices. This trend has resulted in a greater susceptibility to damage arising from the application of excessive voltages such as those caused by an ESD event. During an ESD event, charge is transferred between one or more pins or external electrodes of integrated circuits and another conducting object in a short period of time, typically less than one microsecond. The charge transfer generates voltages large enough to break down insulating films, e.g. gate oxides in MOSFET (MOS Field Effect Transistor) devices, and is capable to dissipate sufficient energy to cause electrothermal failures in the devices. Such failures include contact spiking, silicon melting, or metal interconnect melting. Consequently, in order to deal with transient ESD pulses, an integrated circuit preferably should incorporate protection circuits at every pin.

A lightly doped drain (LDD) extension is commonly used to prevent hot carrier induced degradation in MOS devices. However, transistors with LDD structure are known to have poor ESD performance. Therefore, it is imperative that ESD protection structures are built-in into microelectronic devices.

Offset transistors are commonly used as clamping devices in ESD protection structures. Such offset transistors may be grounded gate n-channel MOS transistors (ggNMOSTs) or gate coupled n-channel MOS transistors (gcNMOSTs). Compared to regular

NMOSTs (with n-LDD), former devices have been shown to be more robust and effective in protecting internal transistors against ESD events. In many cases however, triggering is not fast or effective enough to prevent hard or soft damage from occurring during an ESD event. This is partly due to the fact that the avalanche breakdown voltage Vt1 of protection devices generally does not differ very much from the corresponding breakdown voltage Vt1 of regular NMOSTs, which during an ESD event allows voltage to increase to a level high enough to cause damage in internal circuitry.

All NMOST devices show a so-called snapback behavior during ESD events. Snapback means that a finger of an NMOST switches from MOS action to bipolar action, which enables the finger to conduct large currents at a lower holding voltage.

Fig. 1 shows a schematic diagram of an NMOS offset transistor. Gate, source and drain electrodes are indicated by G, S and D, respectively. In view of the fact that a p-doped substrate is used, a lateral NPN-structure is formed, which results in a parasitic bipolar transistor configuration PT indicated by the dotted transistor symbol. The base electrode of the parasitic bipolar transistor PT is connected via a symbolic substrate resistor RS to a substrate or base electrode B.

Fig. 2 shows a typical I-V characteristic of a grounded gate NMOST (ggNMOST), i.e. an NMOST as shown in Fig. 1 with gate, source and substrate grounded at 0V. When a positive ESD zap, from drain with respect to ground, is applied, the drain voltage rises until it reaches Vt1, at which voltage the n+p-drain-substrate junction undergoes avalanche or first breakdown. The holes, created by impact ionization, will drift towards substrate contact increasing the substrate potential until the source-substrate junction is sufficiently forward-biased to begin bipolar action between drain and source. As a result snapback occurs in the parasitic lateral bipolar NPN transistor and the drain voltage drops to the snapback holding voltage Vsp. As current increases further, thermal or second breakdown occurs at Vt2 marking the onset of permanent damage in the form of increased leakage.

Document US 5,897,348 discloses a method of fabricating salicided CMOS transistors with high ESD resistance. ESD protection devices are fabricated with self-aligned silicide but without LDD. When focussing on the process steps preceding the actual salicidation, the method proposed can be summarized as follows: NMOS offset transistors without n-LDD are used in ESD protection devices. First, a blanket p-LDD ion implantation is performed. Subsequently, an extra blanket phosphorus LATID (Large Angle Tilt

Implanted Drain) ion implant is performed which serves primarily to ensure predominance of n-type dopant in regular NMOST source/drain extensions, while at the same time forming halo anti-punchthrough regions in PMOS devices. The necessity for the former arises from the fact that boron has a higher diffusivity compared to phosphorus. Next, photoresist is patterned such that regular PMOST and ESD protection devices are masked. Then, an n-LDD ion implantation is performed, compensating the p-LDD earlier formed in NMOS device regions. A CVD (Chemical Vapor Deposition) oxide is then deposited and subsequently anisotropically etched back to form spacers. Finally, high dose n+ and p+ source/drain ion implants are performed using photolithography, followed by thermal annealing to activate dopants and form shallow junctions.

However, this known method has several disadvantages: First, it needs an additional phosphorus LATID ion implant. Furthermore, this ion implant causes an increased p-channel series resistance, degrading the current drive capability of the PMOST. Additionally, this increased series resistance may lead to a degradation of the hot-carrier lifetime of the PMOST. Moreover, in ESD protection devices, the blanket phosphorus LATID ion implant partially compensates the "extra" boron originating from the blanket p-LDD ion implant, thus counteracting the desired Vt1 lowering in the ESD protection devices. By the very nature of the large angle ion implant, this partial compensation also occurs at locations where breakdown will take place, i.e. under poly gate edges.

It is therefore an object of the present invention to provide an effective ESD protection at minimal intrusion into an existing process flow and with minimal impact on transistor performance, while at the same time avoiding additional photolithography steps or modifications of existing photo masks.

This object is achieved by a method as claimed in claim 1 and by an integrated circuit arrangement as claimed in claim 11.

Accordingly, the present invention is based on the idea that during an ESD event one would like a protection device to trigger at a lower voltage compared to the more vulnerable regular LDD transistors. By introducing additional dopant in the protection device the avalanche breakdown voltage Vt1 is reduced.

In particular, the protection devices may comprise an offset gate NMOS transistor.

Furthermore, a blanket ion implantation may be used to increase the acceptor concentration. In this case, the blanket ion implantation may be a p-LDD ion implantation. Thereby a mask step can be saved in the process flow. The additional p-type dopant thus introduced in regular LDD NMOS transistors needs to be compensated. This can be done during a preceding donor ion implantation using an appropriate dose. This preceding donor ion implantation may be an n-LDD ion implantation.

As an alternative, a modified p-LDD photo mask may be used to increase the acceptor concentration at the protection devices by using the standard p-LDD ion implantation step for this purpose.

As a further alternative, an additional ESD photo mask may be used to increase the acceptor concentration at the protection devices. The additional ESD photo mask and subsequent ion implantation can be adapted to obtain a clamping effect based on a Zener or avalanche breakdown.

As another alternative, an additional blanket acceptor ion implantation may be performed after formation of an n-LDD structure. The n-LDD ion implantation dose should be high enough to compensate the blanket ESD ion implantation in regular NMOS transistors.

The present invention will now be described in terms of preferred embodiments with reference to the accompanying drawings, in which:

Fig. 1 shows a schematic diagram of a NMOS offset transistor used in ESD protection circuits;

Fig. 2 shows a diagram indicating a typical I-V characteristic of an NMOS offset transistor as shown in Fig. 1, with gate, source and substrate grounded at 0V (ggNMOST);

Fig. 3 shows a flow diagram indicating essential process steps of a forming method according to a first preferred embodiment of the present invention;

Figs. 4A and 4B are cross-sectional views of NMOS and PMOS transistors and ESD protection according to the present invention, showing situations after performing LDD ion implantations (Fig. 4A) and after performing source/drain ion implantations (Fig. 4B);

Fig. 5 shows a flow diagram of replacement steps according to a second preferred embodiment of the present invention;

Fig. 6 shows a flow diagram of replacement steps according to a third preferred embodiment of the present invention; and

Fig. 7 shows a replacement step according to fourth preferred embodiment of the present invention.

The preferred embodiments will now be described on the basis of an integrated semiconductor circuit arrangement comprising a grounded gate NMOST arrangement without n-LDD used as a clamping device in an ESD protection structure.

According to the preferred embodiments, a special measure is taken to ensure that the trigger voltage of internal elements is higher than the trigger voltage of the ESD protection elements. To achieve this, the acceptor concentration is increased at the ESD protection elements to ensure that only the protection elements will snap back.

The breakdown voltage of a pn-junction is to a large extend determined by dopant concentrations. As junction breakdown voltage should well exceed the maximum operating voltage of a device, either p or n region is lightly doped, i.e. $N_A >> N_D$ or vice versa, where N_A and N_D denote acceptor and donor concentrations, respectively. For this type of pn-junctions avalanche breakdown is the dominant mechanism by which voltage breakdown occurs. Since the depletion layer extends much further into the lightly doped region, avalanche multiplication and breakdown processes are most probable in the depletion layer of the lightly doped region. Depletion width decreases with increasing dopant concentration. Thus the junction breakdown voltage can be reduced by increasing the background dopant concentration N_B of the lightly doped region.

Accordingly, by increasing the acceptor concentration N_A in the ESD protection NMOST, the breakdown voltage Vt1 can be reduced.

A p-LDD ion implantation can be used to increase the acceptor concentration in ESD protection devices. Using this method, the trigger or breakdown voltage Vt1 can be reduced by about 2 Volts.

Fig. 3 shows a flow diagram of process steps implemented in the first preferred embodiment. In step S101, n-LDD photolithography is performed to select those areas in which an n-LDD ion implantation is desired. Then, in step S102, n-LDD ion implantation is performed in the desired regions. In particular, the n-LDD ion implantation may be performed using a phosphorus dose sufficient to compensate a later blanket p-LDD ion implantation in the NMOS and ensuring good transistor characteristics as well as hot carrier lifetime. As an example, a dose of 10^{13}-$5x10^{14}/cm^2$ may be used at an energy level of 20-80 keV. The implantation may be performed either at an angle of 0° or a low angle of

about 7° quad mode. Then, in step S103 an n-LDD thermal treatment (i.e. n-LDD drive) is typically performed at a temperature of 800-950°C and a duration of 30-60 minutes.

In step S104 the acceptor concentration in the ESD protection elements is increased using a blanket ion implantation. As an example, the blanket ion implantation may be a p-LDD ion implantation at a dose of about 10^{13}-10^{14}/cm^2 and an energy of 10-25 keV for B+ or an equivalent energy range when using BF_2+. The implantation may be performed either at an angle of 0° or a low angle of about 7° quad mode. As the preceding n-LDD ion implantation has been performed using a dose high enough to compensate the blanket p-LDD ion implantation, additional photolithography is not required in order to increase the acceptor concentration in the ESD protecting elements.

It is noted that the following steps S105 to S110 basically correspond to the respective steps described in the above document US 5,897,348. In step S105, gate sidewall spacers are formed by depositing a dielectric layer using CVD (Chemical Vapor Deposition) technology and subsequent anisotropic etch back. Then, in step S106 an LDD thermal treatment is performed to activate and diffuse the implanted dopants.

Fig. 4A shows a cross-sectional view of the semiconductor circuit arrangement after the LDD ion implantations. As indicated in Fig. 4A, a PMOST, an NMOST and an ESD protection element ESDP, i.e. an additional NMOST without n-LDD, are successively arranged on the semiconductor substrate. The PMOST is arranged in an n-well region NW and the NMOST and the ESD protection element ESDP are arranged in a p-well region PW. The LDD implantation regions are indicated by diagonally hatched layers.

The dominating dopant type (n-type or p-type) is indicated by using different hatching orientations.

Then, in step S107 of Fig. 3, n+ source/drain photolithography is performed followed by n+ source/drain ion implantation in step S108 to thereby form n+ source/drain regions. Subsequently, in step S109 p+ source/drain photolithography is performed, followed by p+ source/drain ion implantation in step S110. Thereby, corresponding p+ source/drain regions are formed.

Fig. 4B shows a cross-sectional view of the semiconductor circuit arrangement after the source/drain regions have been implanted, wherein the vertically hatched region indicates p+ source/drain regions in the n-well region NW and the grid areas indicate n+ source/drain regions in the p-well region PW. Furthermore, the gate sidewall spacers are indicated on both sidewalls of the gate electrode regions.

Fig. 5 shows a flow diagram with steps S104a and S104b according to a second preferred embodiment. Steps S104a and S104b replace the former step S104 of the first preferred embodiment shown in Fig. 3. In step S104a, p-LDD photolithography is performed using a modified p-LDD photo mask, which allows the introduction of p-type dopants in both PMOS transistors and ESD protection elements during the p-LDD ion implantation indicated in step S104b. By using a selective p-LDD ion implantation, as opposed to the blanket implantion used in first preferred embodiment, there is no need to increase the dose of the prior n-LDD ion implantation.

Fig. 6 shows a flow diagram indicating steps S104a to S104d according to a third preferred embodiment, replacing the former step S104 of the first preferred embodiment shown in Fig. 3. In the third preferred embodiment, conventional p-LDD photolithography is performed in step S104a, followed by a p-LDD ion implantation in step S104b. Then, additional photolithography is performed using a dedicated ESD photo mask in step S104c, allowing selective introduction of p-type dopant in ESD protection structures during ESD ion implantation in step S104d. It is noted that said ESD photolithography and ion implantation can be performed at various stages of processing between gate electrode definition and source/drain definition, either prior to or following conventional p-LDD lithography and ion implantation. Also in the third preferred embodiment, the dose of the prior n-LDD ion implantation does not have to be increased. The third preferred embodiment offers full freedom to tailor the breakdown voltage Vt1 of the ESD protection element to a desired lower level.

Fig. 7 shows a flow diagram indicating a replacement step S104' according to a fourth preferred embodiment of the present invention. This fourth preferred embodiment is suitable for processes which have an LDD structure in regular NMOSTs but not in PMOSTs and ESD protection structures. This fourth preferred embodiment, like the preceding preferred embodiments, aims at reducing the breakdown voltage of the ESD protection elements by introducing additional p-type dopant in the ESD protection structures. This can be done prior to spacer definition by using either a blanket or a masked ESD ion implantation. When using a blanket ESD ion implantation process, the dose of the preceding n-LDD implantation should be increased in order to compensate the additional p-type dopant in the regular NMOS transistors, as described in connection with the first preferred embodiment. On the other hand, if a masked ESD ion implantation process is performed, the corresponding remarks of the third preferred embodiment should be considered.

It is noted that the present invention is not restricted to the above preferred embodiments but can be applied in any integrated semiconductor circuit configuration, where a breakdown voltage of an ESD protection element or device is to be reduced. The ESD ion implantation of the second to fourth preferred embodiments may be performed using the specific parameters described in the first preferred embodiment. Furthermore, the acceptor concentration may be increased by introducing any type of suitable dopant material. The preferred embodiments may thus vary within the scope of the attached claims.